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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

MAIL DATE	DELIVERY MODE
12/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,996	HOMEWOOD ET AL.	
	Examiner	Art Unit	
	AURANGZEB HASSAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3-23* is/are allowed.

6)☒ Claim(s) *24,26-28 and 30* is/are rejected.

7)☒ Claim(s) *25 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/23/2009 has been entered.

Allowable Subject Matter

2. Applicant's arguments 11/23/2009 in conjunction with amendments adding limitations that were considered allowable subject matter by the Examiner with respect to newly amended claims 1 - 23, 25 and 29 have been fully considered and are persuasive.

The following is an examiner's statement of additional reasons for allowance: the prior art on the record teaches certain aspects of the current application, involving a stream register unit comprised within a processor arranged to receive and transmit availability functionality for data requests.

However the prior art fails to teach or suggest alone or in combination the limitations structural arrangement in which a processor is linked with a memory bus and communication path to allow for the internal stream register unit to communicate various stall signaling with FIFO functionality coupled to a peripheral. Prior art is further silent

on motivation to combine such features and functionality and is therefore deemed allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statements of Reasons for Allowance."

Claims 1 - 23 allowed.

Claims 25 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis et al (U.S. Patent No. 5,797,043 hereinafter "Lewis") in view of George et al. (US Patent Number 6,785,829, hereinafter "George") further in view of Horning (US Patent Number 5,420,998).

5. As to claim 24, Lewis teaches a system comprising:

a processor comprising an execution for executing instructions; (Host Processor, element 12, figure 1a)

a stream register unit configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral (I/O Channel Controller, element 62, figure 3, element 140, figure 5a), the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral (FIFO pool 172, figure 5a);

a FIFO coupled to the peripheral to receive said first type of data from the peripheral (column 14, lines 25 – 29) and connected to the stream register unit by a communication path (FIFO Pool Bus 144, figures 5a and 6), along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6); and

a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access the second type of data, the second type of data being randomly accessible data held in the data memory (Processor Bus, element 16', figure 2);

wherein the first type of data is supplied via the communication path directly from the FIFO coupled to the peripheral to the stream register unit of the processor (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6) and the second type of data is supplied via the memory bus,

separate from the communication path, between the data memory and the processor (Processor Bus, element 16', figure 2)

wherein the stream register unit is configured to:

in response to a request for a data item from the execution unit, when the data item is located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6).

Lewis fails to teach a system wherein a stream register unit being part of the processor.

George teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of George. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to efficiently optimize a system with regards to real estate in compactness and means of high-speed processing.

The combination of Lewis and George fails to teach system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions.

Horning teaches a system, wherein a processing unit is configured to, when the processing unit does not contain the data item in the next location, request the data item from the memory coupled to the peripheral by setting a "taken" signal across a communication path to a logic high, and when indicated that the data item is not available sending a "valid" signal set to a logic low, send a stall signal to the execution unit, causing the execution unit to stop executing instructions (column 11, lines 5 – 15, when the predetermined level is at empty is considered the point at which the next data item is not available and the system issues a request from the source which is analogous to the peripheral and halts the data transfer which is considered the stall signal which stops the execution of the transfer instruction).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above teachings of Horning. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system (column 5, lines 11 – 18).

6. Claim 26 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of Garcia et al. (US Patent Number 6,433,785 hereinafter "Garcia") further in view of George.

7. As per claims 26 and 30, Lewis teaches a stream register being part of a processor comprising an execution unit, the stream register being connectable between

the execution unit and peripheral and between the execution unit and a memory, comprising:

a receiver arranged to receive a request for a data item from the execution unit (column 10, lines 30 - 41); at least one FIFO configured to store the data item received form the peripheral (FIFO pool 172, figure 5a); and

a stream engine (element 76, figure 3), arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item (I/O Channel Controller, element 62, figure 3), and, when the data item is available (available space and data, Table VII sent via BTU, element 170 figure 5b.), send the data item to the execution unit of the processor.

Lewis fails to teach a register wherein when the data item being requested is not available, sending a timeout signal to the processor.

Garcia teaches a register wherein when the data item being requested is not available, sending a timeout signal to the execution unit of the processor (timeout counter, column 5, lines 26 – 42), (as per claim 30) wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, when the data item subsequently becomes available (posted write buffer available signal 350, column 5, lines 30 – 31), receive a signal instructing it to cease sending the timeout signal, and to upon receipt of the said instruction cease sending the timeout signal to the processor (column 5, lines 26 – 42).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Garcia.

One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to optimize a request process in which resources are valuable and delays need to be minimized, improving processor to device throughput.

Lewis/Garcia fails to teach a system wherein a stream register unit being part of the processor.

George teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis/Garcia with the above teachings of George. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to efficiently optimize a system with regards to real estate in compactness and means of high-speed processing.

8. As to claim 27, Lewis teaches a stream register, wherein the stream engine is arranged to send the timeout signal to the execution unit of the processor after a predetermined period of time (Interrupt, table III).

9. As to claim 28, Lewis teaches a stream register, wherein the stream engine is further arranged to, when the data is available, temporarily store the data in a register

file for access by the execution unit of the processor (temporarily stored in a FIFO within the bus master units, column 19, lines 52 – 63).

Response to Arguments

10. Applicant's arguments filed 11/23/2009 with respect to claims 24, 26 - 28 and 30 have been fully considered but they are not persuasive.

The Applicant argues limitations of the preamble to overcome the prior art for which the Examiner has provided additional citations to better understand the rejection in view of the prior art. Furthermore the Applicant argues limitations of the stall signal functionality with respect to a predetermined amount of time. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The prior art teaches a stall signal as necessitated by the claims and there are no claim limitations which would preclude the prior art from such capable functionality.

The Applicant is invited to contact the Examiner to discuss the allowable subject matter described.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AURANGZEB HASSAN whose telephone number is (571)272-8625. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on 571-272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182